REMARKS

This application has been carefully considered in connection with the Examiner's Action. Reconsideration and allowance are respectfully requested in view of the following.

Claims 1 and 11 have been amended to better describe the subject matter regarded as the invention. Claims 8, 9 and 15 have been amended for consistency purposes and/or to depend upon a pending claim. Claims 7, 12, 14, 17, 19 and 20 have been canceled without prejudice or disclaimer. Finally, new Claims 21-27, all of which are directed to further embodiments of the 7nvention deemed patentable over the art of record, have been added.

Claims 1 and 2 stand rejected under the judicially created doctrine of nonstatutory double patenting as being anticipated by Claim 1 of U.S. Patent No. 6,667,636 to Sihlbom et al. Claims 1, 3, 6, 11 and 18-20 stand rejected under 35, U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,263,390 to Alasti et al. Claims 1-3, 6 and 19-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,041,000 to Ozcelik et al. Claims 2 and 13 stand rejected under 35 U.S.C. § 103(a) as being obvious over Alasti et al. in view of Ozcelik et al. Claims 7 and 14 stand rejected under 35 U.S.C. §103(a) as being obvious over Alasti et al. in view of U.S. Patent No. 6,412,027 to Amrany et al. Claims 4-5, 8-10, 12, 15-16 and 18 stand rejected under 35 U.S.C. § 103(a) as being obvious over Alasti et al. or, in the alternative, obvious over Alasti et al. in view of Amrany et al. Claim 17 stands rejected under 35 U.S.C. § 103(a) as obvious of Alasti et al. in view of Amrany et al. and further in view of Ozcelik et al. Claims .3-6, 11-13 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozcelik et al. in view of U.S. Patent No. 6,263,390 to Normoyle et al. Claims 7-10 and 14-17 stand rejected under 35 U.S.C. § 103(a) as obvious over Ozcelik et al. in view of Amrany et al. Finally, Claims 8-10 and 15-17 stand rejected under 35 U.S.C. § 103(a) as obvious over Ozcelik et al. in view of Amrany et al. and further in view of Normoyle et al.

In response, the Applicants respectfully traverse the various rejections of Claims 1-20and instead submits that Claims 1-6, 8-11, 13, 15-16 and 18, as above amended, as well as newly added Claims 21-27, are neither taught nor suggested by the art of record. Accordingly, the Applicants respectfully request the reconsideration and withdrawal of the various rejections of Claims 1-20 and the allowance 1-6, 8-11,13, 15-16, 18 and 21-27. Arguments in support of Applicants' position that the claims, as presented herein, are patentable over the applied references shall now be set forth with the specificity required by 37 C.F.R. § 1.111(b).

With respect to the nonstatutory double patenting rejection of Claims 1 and 2 as anticipated by Claim 1 of U.S. Patent No. 6,667,636 (the '636 Patent), the Applicants respectfully submit that Claims 1 and 2, as above amended, no longer have each and every element of Claim 1 of the '636 Patent. It is further believed that application of an anticipatory and/or obviousness-type double patenting rejection of either original Claims 1-6, 8-11, 13, 15-16, and 18, as above amended, or new Claims 21-27, as herein presented, in view of the '636 Patent is not appropriate. In this regard, it is noted that, while the claims pending in the present application and the claims issued in the '636 Patent bear certain similarities, it is further noted that the claims pending in the present application diverge in a number of key aspects from the claims issued in the '636 Patent. For example, the pending claims recite, in varying specificity, that the claimed sharing units are adapted to receive data from separate and discrete external devices. As a result, Applicants' invention are directed to various embodiments of an integrated circuit configured to alternately transmit data originating from discrete external devices to a memory coupled to a digital signal processor. Such a limitation, which is presented to the examiner as purely exemplary of the distinctions between the pending claims and the claims of the '636 Patent, is neither recited nor suggested by the claims of the '636 Patent. Accordingly,

the Applicants respectfully request the reconsideration and withdrawal of the double patenting rejection of Claims 1 and 2.

As to the plural art rejections applied against various ones of original Claims 1-20, the Applicants respectfully submit that all but one of the rejections have been rendered moot in light of the amendment to the claims presented herein. More specifically, the undersigned believes that the sole rejection which remains pertinent to the pending claims is the Examiner's rejection of Claims 7 and 14 under 35 U.S.C. § 103(a) as obvious over Alasti et al. in view of Amrany et al. In this regard, it is noted that Amrany et al. was cited as disclosing "a cascaded DMA controller configuration to accommodate multiple DMA devices[,] each DMA controller having built in arbitration circuitry to avoid having a separate arbitration circuit" and that each of the pending claims recite structure that the Examiner would assert as being a variant of the "cascading DMA controller configuration" that the Examiner asserts is taught by Amrany et al.

In response to this actual and/or prospective assertion of the teachings of Amrany et al., the Applicants respectfully submit that Amrany et al. neither teaches nor suggests, either alone or in combination with one or more of the cited references, Applicants' invention as defined by Claims 1-6, 8-11,13, 15-16, 18 and 21-27, as above amended. More specifically, the Applicants note that the multiple digital memory access controllers (DMACs) 130, 132 and 134 disclosed by Amrany et al. are both coupled and function differently than the first and second sharing units disclosed and claimed by the Applicants. More specifically, the DMACs 130, 132 and 134 are coupled to a common source memory, presumably, for handling of plural reads therefrom. In contrast, the sharing units are adapted for coupling to discrete external devices in such a way that data originating at a first external device that may require pre-processing by the first and second programmable logic cores (PLCs) before processing by the digital signal processor (DSP) may be propagated to the PLCs without interfering with the propagation of data originating at a

second external device to the DSP. Such a configuration is neither taught nor suggested by the cited art.

For all the above reasons, the Applicants respectfully request the reconsideration and withdrawal of the various rejections of Claims 1-20, the allowance of Claims -6, 8-11,13, 15-16, 18 and 21-27, as above amended, and the passing of this application to issue.

This application is now considered to be in condition for allowance. A prompt Notice to that effect is, therefore, earnestly solicited.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 12-2252, LSI Logic Corporation.

Respectfully submitted,
CONLEY ROSE, P.C.

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